devices located on the first side, the top active optical devices also being on the first side, with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

creating sidewalls defining openings in the substrate extending from the active device contacts on the first side through the substrate to a bottom side of the substrate opposite the first side at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

5. (Amended) The method of claim 1 further comprising:

removing the carrier after the connecting.

6. (Amended) The method of claim 1 wherein the connecting comprises:

patterning traces between the points and the locations correspondingly aligned with the at least some electronic chip contacts, and

making the traces electrically conductive.

7. (Amended) The method of claim 6 wherein the patterning traces comprises:

patterning at least some of the traces on the substrate and at least some other of the traces on the electronic chip.

8. (Amended) The method of claim 6 wherein the patterning traces further comprises:

patterning traces on the electronic chip.

13. (Amended) A method of connecting two chips, one of which being a topside active chip, each of the two chips having electrically corresponding contacts to be joined together that are physically mismatched in alignment relative to each other, the method comprising:

creating electrically conductive paths on an insulator surface of the topside active chip, each of the electrically conductive paths extending between physical locations of device contacts of one of the two chips and physical locations of the electrically corresponding contacts on the other of the two chips, from the device contacts through the topside active chip to the physical locations of the electrically corresponding contacts.

14. (Amended) The method of claim 13 wherein the insulator has holes defined by sidewalls, extending from the device contacts through the insulator, and the creating the electrically conductive paths comprises:

making the holes electrically conductive.

17. (Amended) The method of claim 13 further comprising:

joining the two chips.